



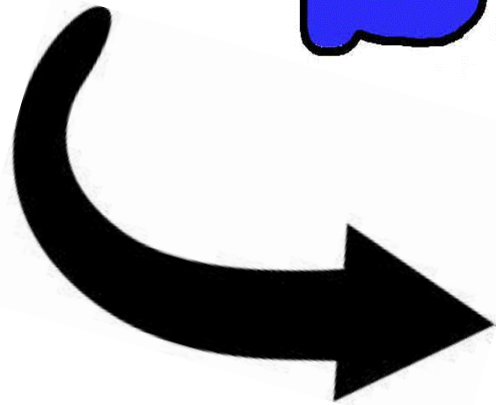
Jason Power
UW-Madison

I ♥ gem5





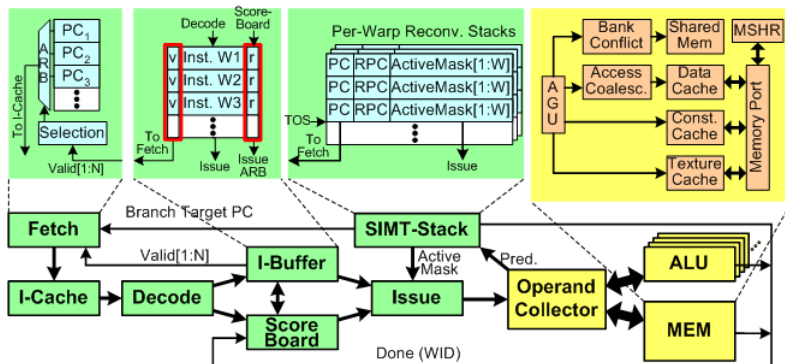
Outline



My story

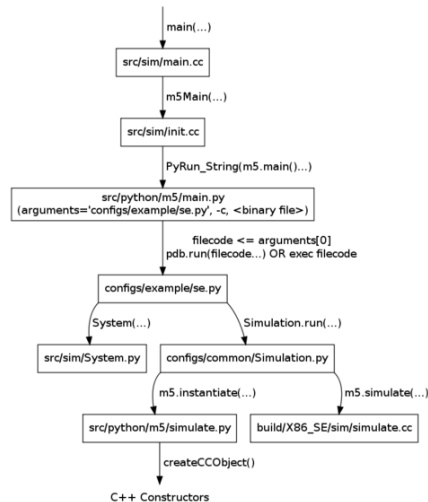
gem5GPU

GPGPU-Sim

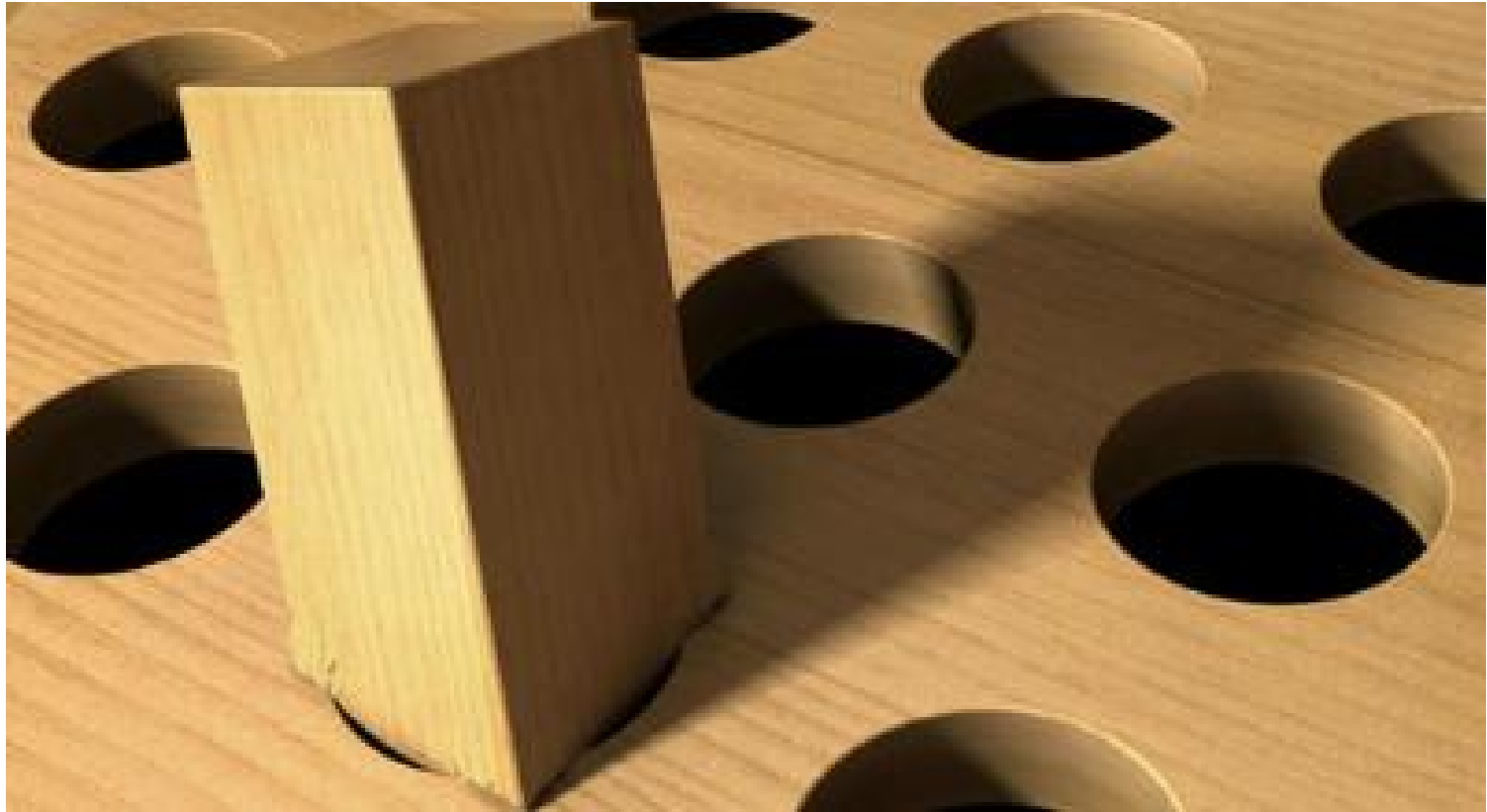


gem5

Function Call Sequence for gem5 "Hello, World" Example



Merges are hard



Merges are difficult

Pointless name changes

```
- out_port(reqToDirectory_out, RequestMsg, reqToDirectory,  
desc="...");  
+ out_port(requestToDir_out, RequestMsg, requestToDir, desc="...");
```

Functions disappear

```
- Packet::reinitFromRequest()  
- {  
-     assert(req->hasPaddr());  
-     . . .  
- }
```


Merges are difficult

Ruby backing store



Checkpointing



O3 CPU and Ruby:

Merges are difficult

JAN

S	M	T	W	T	F	S
			1	2	3	4
5	6	7	8	9	10	11
12	13	14	15	16	17	18
19	20	21	22	23	24	25
26	27	28	29	30	31	

Sisyphean task



10-4



Story of a new user



JORGE CHAM © 2009

```
normal
File Edit View Search Terminal Help

arch:
alpha/ arm/ generic/ isa_parser.py* isa_parser.pyc micro_asm.py micro_asm.pyc micro_asm_test.py* mips/ null/ power/ SConscript sparc/

base:
addr_range.hh bigint.cc bitunion.hh circlebuf.cc cp_annotate.hh date.cc flags.hh inet.hh loader/ output.cc
addr_range_map.hh bigint.hh callback.cc circlebuf.cc CPA.py debug.cc hashmap.hh inifile.cc match.cc output.hh
atomicio.cc bitfield.hh callback.cc compiler.hh cprintf.cc debug.cc hostinfo.cc inifile.hh match.hh pollevent.cc
atomicio.hh bitmap.cc cast.hh condcodes.hh cprintf_formats.hh fenv.c hostinfo.hh intmath.cc misc.cc pollevent.hh
barrier.hh bitmap.hh chunk_generator.hh cp_annotate.cc cprintf.hh fenv.hh inet.cc intmath.hh misc.hh printable.hh

cpu:
activity.cc checker/ dummy_checker.hh func_unit.hh inteltrace.cc minor/ pc_event.hh reg_class.hh
activity.hh CheckerCPU.py DummyChecker.py FuncUnit.py inteltrace.hh nativetrace.cc pred/ SConscript
base.cc cpuevent.cc exec_context.cc loader/ nativetrace.hh profile.cc simple/
BaseCPU.py cpuevent.cc exec_context.cc inst_pb_trace.cc intr_control.hh ncpu/ profile.hh simple_thre
base_dyn_inst.hh CPUTracers.py exetrace.cc inst_pb_trace.hh intr_control_noisa.cc o3/ quiesce_event.cc simple_thre
base_dyn_inst_impl.hh decode_cache.hh exetrace.hh InstPBTrace.py IntrControl.py op_class.hh quiesce_event.hh sat.hh
base.hh dummy_checker.cc func_unit.cc inst_seq.hh kvm/ pc_event.cc reg_class.cc static_inst

dev:
alpha/ copy_engine.hh dma_device.hh etherint.cc etherpkt.hh ide_ctrl.cc intel_8254_timer.hh mips/
arm/ CopyEngine.py etherbus.cc etherint.hh etherptap.cc ide_ctrl.hh io_device.cc ns_gige.cc
baddev.cc Device.py etherbus.hh etherptap.hh ide_disk.cc io_device.hh ns_gige.hh
baddev.hh disk_image.cc etherdevice.cc etherlink.hh ide_disk.hh isa_fake.cc ns_gige_reg.h
BusDevice.py disk_image.hh etherdevice.hh ethernet.py ide_py 18254xGbE_defs.hh ide_py isa_fake.hh pciconfigall.cc
copy_engine.cc DiskImage.py etherdump.cc etherobject.hh ide_wdcreg.hh ide_wdcreg.h mc146818.cc pciconfigall.hh
copy_engine_defs.hh dma_device.cc etherdump.hh etherpkt.cc ide_atareg.h intel_8254_timer.cc mc146818.h pcidev.cc

doc:
inside-minor.doxygen memory_system.doxygen

doxygen:
footer.html images/ stl.hh

kern:
kernel_stats.cc kernel_stats.hh linux/ operatingssystem.cc operatingssystem.hh SConscript solaris/ system_events.cc system_events.hh tru64

mem:
abstract_mem.cc coherent_xbar.cc dramsim2.cc ExternalSlave.py MemObject.py packet.hh port_pro
abstract_mem.hh coherent_xbar.hh dramsim2.hh fs_translating_port_proxy.cc mport.cc packet_queue.cc protocol
AbstractMemory.py com_monitor.cc DRAMSIM2.py mem_checker.cc multi_level_page_table.cc packet_queue.h request_
addr_mapper.cc com_monitor.py dramsim2_wrapper.cc mem_checker.cc multi_level_page_table.cc page_table.cc ruby/
AddrMapper.py dram_ctrl.cc dram_ctrl.cc external_master.cc mem_checker_monitor.cc multi_level_page_table_impl.hh physical.cc SConscri
bridge.cc dram_ctrl.hh ExternalMaster.py mem_checker_monitor.hh noncoherent_xbar.cc port.cc se_trans
bridge.hh DRAMCtrl.py external_slave.cc mem_checker_monitor.hh noncoherent_xbar.cc port.cc simple_m
Bridge.py drampower.cc external_slave.hh mem_object.cc mem_object.cc packet_access.hh port.hh simple_m
cache/ drampower.hh external_slave.hh mem_object.cc mem_object.cc packet.cc port_proxy.cc

proto:
inst.proto packet.proto protoio.cc protoio.hh SConscript
```



WWW.PHDCOMICS.COM

No info for beginning users

n26001482 via gem5-users | 6 Dec 14:55 2014

How and when to use the python?

Hi, all.

I found some Python files in the gem5/configs/common

But I don't understand how and when to use them.

So far the Python file I used is either se.py or fs.py.

Could anyone tell me?

Thanks a lot!

BEST

M.Y.

gem5-users mailing list

gem5-users <at> gem5.org

<http://m5sim.org/cgi-bin/mailman/listinfo/gem5-users>

Defaults are confusing

```
116 parser.add_option("--l1i_size", type="string", default="32kB")
117 parser.add_option("--l2_size", type="string", default="2MB")
118 parser.add_option("--l3_size", type="string", default="16MB")
119 parser.add_option("--l1d_assoc", type="int", default=2)
120 parser.add_option("--l1i_assoc", type="int", default=2)
121 parser.add_option("--l2_assoc", type="int", default=8)
122 parser.add_option("--l3_assoc", type="int", default=16)
123 parser.add_option("--cacheline_size", type="int", default=64)
124
```

Which trumps?

```
57 class L2Cache(BaseCache):
58     assoc = 8
59     hit_latency = 20
60     response_latency = 20
61     mshrs = 20
62     tgts_per_mshr = 12
63     write_buffers = 8
```

Defaults are confusing

```
113 parser.add_option("--num-l2caches", type="int", default=1)
114 parser.add_option("--num-l3caches", type="int", default=1)
115 parser.add_option("--l1d_size", type="string", default="64kB")
116 parser.add_option("--l1i_size", type="string", default="32kB")
117 parser.add_option("--l2_size", type="string", default="2MB")
118 parser.add_option("--l3_size", type="string", default="16MB")
```

```
92 for i in xrange(options.num_clusters):
93     for j in xrange(num_cpus_per_cluster):
94         #
95         # First create the Ruby objects associated with this cpu
96         #
97         l0i_cache = L0Cache(size = '4096B', assoc = 1, is_icache = True,
98                             start_index_bit = block_size_bits, replacement_policy="LRU")
99
100         l0d_cache = L0Cache(size = '4096B', assoc = 1, is_icache = False,
101                             start_index_bit = block_size_bits, replacement_policy="LRU")
102
```

Defaults are confusing

```
110 parser.add_option("--l2cache", action="store_true")
111 parser.add_option("--fastmem", action="store_true")
112 parser.add_option("--num-dirs", type="int", default=1)
113 parser.add_option("--num-l2caches", type="int", default=1)
114 parser.add_option("--num-l3caches", type="int", default=1)
115 parser.add_option("--l1d_size", type="string", default="64kB")
116 parser.add_option("--l1i_size", type="string", default="32kB")
117 parser.add_option("--l2_size", type="string", default="2MB")
118 parser.add_option("--l3_size", type="string", default="16MB")
119 parser.add_option("--l1d_assoc", type="int", default=2)
120 parser.add_option("--l1i_assoc", type="int", default=2)
121 parser.add_option("--l2_assoc", type="int", default=8)
122 parser.add_option("--l3_assoc", type="int", default=16)
123 parser.add_option("--cacheline_size", type="int", default=64)
124
```

**No L3 caches are ever
created!!**

Et cetera

Ignore mailing list

December 2014: 41 f... 10... ..

Inconsistencies

See blog post

```
{  
+ Y[i];
```

Division
unit

	Latency	Issue rate	x86 perf	ARM perf
Config 1	10	10	1.0x	8.0x
Config 2	10	1	1.0x	9.6x (1.2x)

Expect nearly 10x

The slide features a solid blue background. On the left and right edges, there are decorative patterns of overlapping chevron shapes in yellow, magenta, and light blue. The text is centered in the upper half of the slide.

Addressing the “horrors”

Solutions

Merging
headaches



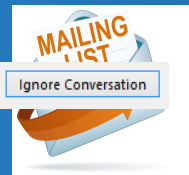
➤ API Freezes & Improved regression coverage

Configuration
complexity



➤ Fewer command-line options & more scripts

Lack of new user
documentation



➤ Better documentation: gem5 for dummies

Community Organization

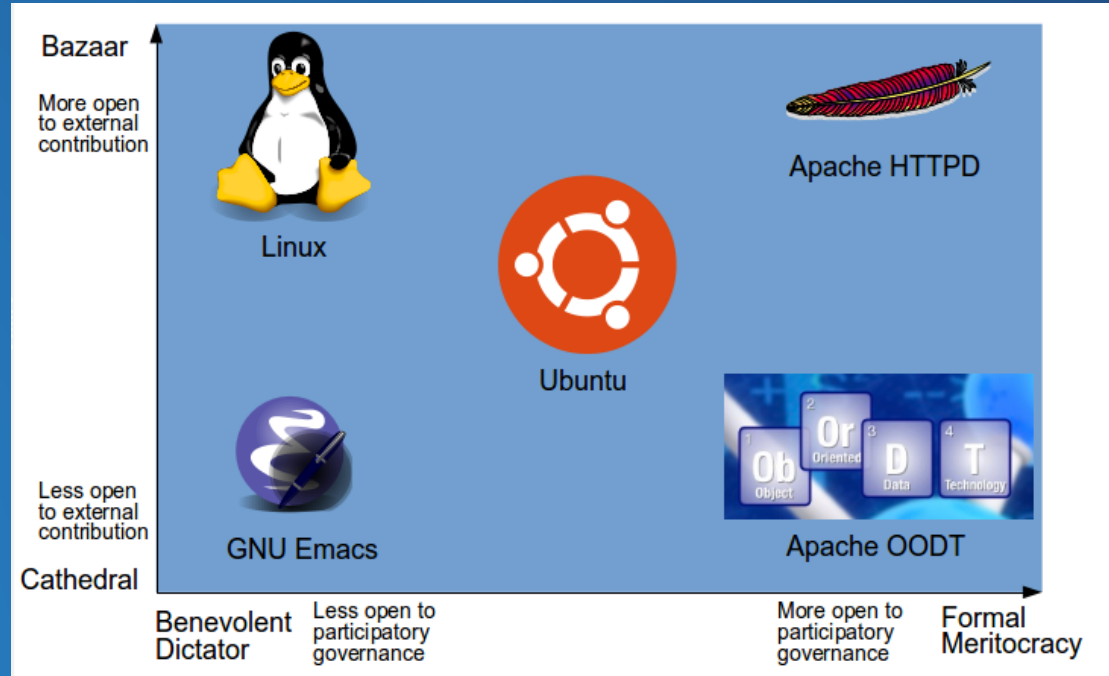


Linux



PostgreSQL

Community Organization



gem5 Foundation



Advisory board



Conclusions



Discussion?



Backup/other slides

More money

Don't make a PhD student do it
An architect isn't the right person

We need to *pay* a real software developer

New



Ignore mailing list

December 2014: 41 threads, 18 with no replies



Ignore mailing list

March 16, 2014:

Hi all! I encounter the error as following when I simulate ruby_fs.py on ALPHA...

March 17, 2014:

I am also facing the assertaion error which is described by

September 16, 2014:

I am using the latest stable version for x86+ruby+FS. I encountered the same assertion failure as the following email (posted in May)

January 6, 2015:

I recently ran into this and I saw several previous messages on the list about it without replies, so I figured I'd post a workaround (I'm not sure of the best way to do a real fix).

Merges are difficult

SLICC



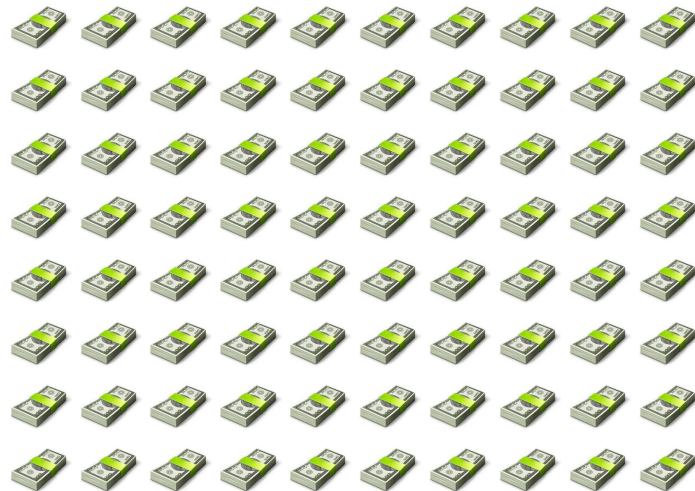
Config files are complicated

More than 4000 lines of code in configs/

16 person-months



\$250,000



Inconsistencies

Program:

```
for (int i = 0; i < N; i++) {  
    Y[i] = X[i] / alpha + Y[i];  
}
```

Division
unit

	Latency	Issue rate	x86 perf	ARM perf
Config 1	10	10	1.0x	8.0x
Config 2	10	1	1.0x	9.6x (1.2x)

Expect nearly 10x

Code isn't contributed back

the grail



30 seconds

gem5 Foundation

